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IN THE SPECIFICATION

Please amend the paragraphs identified in the electronically filed application to read as follows:

[0005] The FET transistor 17 includes a drain region D, a source region S, and a channel CH. The drain region D is located in an N+ doped bit line diffusion (XA) region 26 on top of the substrate 15. The source region S is formed in an N+ doped outdiffusion region OD, which is juxtaposed with an N+ doped strap 13 formed in the deep trench DT, at the top of an N+ doped capacitor node 11. The channel CH of the FET transistor 17 is located in the P- doped substrate 15 to the left of the gate oxide layer 24 formed along the upper sidewall of the [[of the]] deep trench DT, with the channel region CH of transistor 17 located between the drain region D and the source region S, from top to bottom. Thus the channel CH and the gate conductor 16 are separated, as stated above, by the thin gate oxide layer 24, which is formed on the sidewall of the deep trench DT with the drain region D at the top of the channel CH and the source region S at the bottom of the channel CH in the vertical transistor 17. The transistor 17 is turned on when the gate conductor (GC) 16 is raised to V_{pp} by electrical connection of wiring thereto (not shown) at the top of the GC 16.

[0007] The deep trench capacitor C (comprising a three-dimensional structure), which is formed in the lower portion of the deep trench DT, is used as the charge storing capacitor C of the MOSFET cell 10. As will be well understood by those skilled in the art, such a deep trench capacitor C is normally formed by the process of etching vertical deep trenches DT of various dimensions into a semiconductor substrate, such as doped silicon substrate 15. As usual, the bottom[[s]] of the deep trench DT contains N+ doped polysilicon, which serves as the storage node 11 of the capacitor C, with the storage node 11 comprising the inner plate of the capacitor C separated from the substrate 15 by dielectric layers 12/44. The bottom of the deep trench DT is shown with intermediate portions cut away near the bottom of FIG. 1A.

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[0016] One of the problems with previous designs of the vertical pass transistors 17 was that there was a large substrate bias effect that degraded the write back current. A graded doping profile in the direction perpendicular to the channel CH is required to achieve a small substrate bias effect. In the planar pass transistor design, this is naturally achieved with a blanket Vt adjustment implant.

[0023] Referring to FIG. 2C, there is also a solid, ~~[[line]]~~ vertically graded profile line of P-type dopant 18P'' produced by the process illustrated by FIG. 2A. The cell 10 is shown after the process of angled ion implantation of dopant atoms performed in FIG. 2A has resulted in vertical scattering of the implanted dopant atoms combined with diffusion in the region of the channel CH and therebelow, which creates a vertically graded profile 18P'' (from top to bottom) of P-type dopant atoms as shown in FIG. 2(with a peak spaced on the right near the gate oxide layer 24 a preferred distance "m" below the line 25 at the bottom of the XA region 26 trailing down to substantially lower concentrations thereabove and therebelow.

[0024] However, FIG. 2C also shows a hypothetical dotted profile line of a graded vertical profile of P-type dopant 18P'' caused by too shallow a recessing of the gate conductor 16. If the actual depth of the recessed gate conductor 16 is at the level of the hypothetical dotted line level 30, a distance n above the level 40, then as shown by the dotted line curve 18P'' in FIG. 2C, the result will be that the maximum of the vertical profile of the P-type dopant will be only the distance m-n below the line 25, which is too close to the lower boundary 25 of the XA region 26. That is undesirable since the Vt implant will be too high, i.e. in too close proximity to the drain region D in XA region 26, ~~[[.]]~~ and P-type dopant will be compensated by N+ dopant atoms in the region 26. Thus the deep trench vertical DRAM processes can be faced with additional Vt variation due to problems in controlling the actual depth of the gate recess level 40.

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[0030] Copending, commonly assigned, U.S. patent application (~~Attorney Docket No. FIS9-2002-0015~~) of Dureseti Chidambarrao et al. entitled "Vertical MOSFET with Horizontally Graded Channel Doping", Serial No.: 10;096,219; filed 11 March 2002, now U.S. patent No. 6,740,920 describes body effects in vertical MOSFET transistors which are considerably reduced with other device parameters unaffected wherein the vertical transistor has a threshold implant with a peak at the gate and an implant concentration distribution that declines rapidly away from the gate to a plateau having a low P-well concentration value. In one embodiment two body implants both of which involve counterdoping are employed with an angled ion implantation having a peak at the gate that sets the V_t and a laterally uniform low dose implant that sets the well dopant concentration.

[0034] Further in accordance with this invention, a method is provided for formation of a trench vertical transistor in a semiconductor substrate having a surface and a trench with a sidewall formed in said semiconductor substrate. The semiconductor substrate is doped with a dopant, a counterdoped drain region in the surface of said substrate and a channel along-side said sidewall, said drain region having a top level and a bottom level, a counterdoped source region formed in the substrate juxtaposed with said sidewall below said channel, a gate oxide layer formed on the sidewalls of said trench, and a gate conductor formed in said trench. The method includes the following steps. Recess the gate conductor below the surface of the semiconductor substrate. Perform angled ion implantation at an angle $\theta + \delta$ with respect to vertical of a counterdopant into the channel below the location of the drain region. Perform angled ion implantation at an angle θ with respect to vertical of a dopant into the channel below the location of the drain region.

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[0036] Further in accordance with this invention, a method is provided for formation of a deep trench vertical transistor in a semiconductor substrate having a surface and a trench with a sidewall formed in the semiconductor substrate, the deep trench including a deep trench capacitor filled with a node, a strap, a collar and a node dielectric lining the deep trench, and a buried plate formed in the semiconductor substrate surrounding the deep trench, the semiconductor substrate being doped with a dopant, a counterdoped bit line diffusion region in the surface of the substrate and a channel alongside the sidewall, the bit line diffusion region having a top level and a bottom level, a counterdoped source region formed in the substrate juxtaposed with the sidewall below the channel, a gate oxide layer formed on the sidewalls of the trench, and a gate conductor formed in the trench. The method includes the following steps. Recess the gate conductor below the surface of the semiconductor substrate. Perform angled ion implantation at ~~[[an]]~~ a greater angle $\theta + \delta$ with respect to vertical of a counterdopant into the channel below the location of the drain region and perform angled ion implantation at ~~[[an]]~~ a lesser angle θ with respect to vertical of a dopant into the channel below the location of the bit line diffusion region. Preferably, the recessing of the gate conductor reaches below the bottom level of the bitline diffusion region.

[0038] ~~forming~~ Form a deep trench having a top and a lower portion in a doped semiconductor substrate. ~~[[,]]~~ ~~forming~~ Form a counterdoped buried plate in the substrate surrounding the lower portion of the deep trench. ~~[[,]]~~ ~~forming~~ Form a storage node dielectric layer as a conformal thin film on inner walls of the deep trench. ~~[[,]]~~ ~~filling~~ Fill the deep trench with an initial storage node conductor which is counterdoped. ~~[[,]]~~ ~~recessing~~ Recess the initial storage conductor. ~~[[,]]~~ ~~forming~~ Form a dielectric collar as a conformal film on exposed inner walls of the deep trench with the dielectric collar recessed below the top of the deep trench. ~~[[,]]~~ ~~filling~~ Fill the deep trench with a complementary storage node conductor which is counterdoped above and in contact with the initial storage conductor. ~~[[,]]~~ ~~recessing~~ Recess the complementary storage node conductor to a buried strap level in the deep trench. ~~[[,]]~~ ~~forming~~ Form a counterdoped buried strap counterdoped outdiffusion by

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diffusion of dopant from the complementary storage node conductor into the substrate. ~~[[,]]~~
~~forming Form~~ a trench top oxide layer over the complementary storage node conductor. ~~[[,]]~~
~~forming Form~~ a gate oxide layer which is conformal with exposed inner walls of the deep
trench. ~~[[,]]~~ ~~forming Form~~ a gate conductor in the deep trench above the trench top oxide
layer. ~~[[,]]~~ ~~recessing Recess~~ the gate conductor below the bottom surface of the bit line
diffusion region. ~~[[, and]]~~ ~~performing Perform~~ angled ion implantation at ~~[[an]]~~ a greater
angle $\theta + \delta$ with respect to vertical of a counter-dopant into the channel below the location of
the bit line diffusion region and ~~performing perform~~ angled ion implantation at ~~[[an]]~~ a lesser
angle θ with respect to vertical of a dopant into the channel below the location of the drain
region. Preferably, the lesser angle θ is about 7° and the greater angle $\theta + \delta$ is about 30° ; the
counterdopant is selected from the group consisting of arsenic and phosphorus; and/or the
counterdopant comprises arsenic ions implanted at an energy of about 10 keV.

[0039] The foregoing and other aspects and advantages of this invention are explained and
described below with reference ~~[[tothe]]~~ to the accompanying drawings, in which:

[0042] FIG. 2A illustrates a solution to the problem of the process of ~~[[FIB.]]~~ FIG. 1B, which
is to perform ~~[[on]]~~ on the cell of FIG. 1A V_t adjustment by an angled ion implantation of P
type dopant ions into and through a recessed gate conductor composed of N^+ doped
polysilicon.

[0045] FIG. 2D shows a desirable composite “three-dimensional” profile (vertical and
horizontal distribution) of the concentration levels of the p type dopant atoms implanted in
the step illustrated by FIG. 2A with the gate conductor~~[[6]]~~ recessed to the level shown in
FIGS. 2A and 2B.

[0047] FIG. 3~~[[.]]~~ illustrates a device structure and the V_t adjustment implant process in
accordance with this invention.

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[0050] FIG. 3 illustrates a device structure and the V_t adjustment implant process in accordance with this invention with the N^+ doped bit line ~~diffusion~~ diffusion XA region 26 shown at the top of the semiconductor substrate 15 while angled ion implantations 32 and 34 are being performed. It is possible that the XA region 26 is formed later in the manufacturing process, but the resulting channel doping levels are the same.

[0051] In accordance with this invention, ~~[[The]]~~ the solution to the problem of FIGS. 2C and 2E is illustrated by FIG. 3 in which a V_t adjustment by an angled ion implantation of P-type dopant 32 has been provided into the recessed gate electrode 16 composed on N^+ doped polysilicon implanted at the lesser angle θ with respect to vertical and the lateral scattering of the energetic ions combined with diffusion creates a laterally graded profile as illustrated by dopant profile 18P" or 18P" in FIG. 2C combined with an implant of N-type dopant ions 34 at ~~[[an]]~~ a greater angle ~~[[$\theta - \delta$]]~~ $\theta + \delta$ with respect to vertical which compensates for P-type ions implanted into the channel CH just below the drain region D. While relatively heavy P-type doping into the channel below the drain region D is needed to suppress the sub- V_t leakage, as explained above, it must not be substantial near the drain region CH. On the other hand, a P-type doping level near the buried strap out-diffusion region OD needs to remain low since high doping level leads to excessive junction leakage. As a result, it is also advantageous to dope the channel region non-uniformly in the vertical direction.

[0052] With the process of this invention, the pass transistor XA 26 junction is defined by implant energy only and is self-aligned to the recessed gate edge ~~regardless~~ regardless of the gate recess variation. It has been found that V_t variation can be greatly reduced while the channel length can be further scaled down by about 50 nm.

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[0054] (1) starting with a silicon substrate 15, a pad structure 38 consisting of a thin thermal oxide (2-20nm) is grown on the silicon substrate 15; a deposited pad masking layer 59 composed of silicon nitride (50-200nm), and a layer of densified TEOS oxide (or HDP oxide) (50-500nm). Then a top layer of BSG oxide (50-500nm) [[then]] is deposited.

[0056] (3) [[A]] An N+ counterdoped buried plate 42 is formed by diffusion of N-type dopant through the lower portion of the deep storage trench DT into the surrounding region of the substrate 15, using anyone of a number of well known methods (e.g. out-diffusion from an ASG glass, gas phase doping and the like).

[0057] (4) A conformal storage node dielectric layer 44 composed of silicon oxide is formed as a thin film on [[with]] the inner walls of the deep trench DT.

[0058] (5) The deep trench DT is filled with N+ doped polysilicon forming the lower portion of the storage node 11 which is then recessed to form a conformal polysilicon buffered LOCOS collar 12 on the inner walls of the deep trench DT [[()]] or other type of dielectric collar 12 above the storage node dielectric layer 44 and the lower portion of the storage node 11 in the upper portion (approximately top 1 micrometer). The upper portion of the sidewalls of the deep trench DT remain exposed to the P-doped silicon substrate 15 leaving the top of the dielectric collar 12 recessed well below the top of the deep trench DT.

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[0060] (7) A standard buried-strap process is used to form a buried strap out-diffusion region OD in the P-doped silicon substrate 15 by buried strap out-diffusion of N type dopant from the N+ polysilicon in strap 13 through the sidewall of the deep storage trench. The standard strap process includes the removal of the collar oxide 12 from the side of the deep trench DT above the point at which the strap 13 is to be formed, and the deposition and etching of the doped strap polysilicon 13. The strap polysilicon 13 electrically bridges the N+ doped polysilicon of the storage node 11 in the deep trench DT (storage node electrode of the capacitor) to the P-doped, single crystal silicon substrate 15 adjacent to the deep storage trench. A buried strap N+ doped out-diffusion region OD is subsequently formed by buried strap out-diffusion of the N type dopant from N+ doped polysilicon strap 13 in the course of processing at elevated temperatures.

[0062] (9) A conformal thin film of silicon oxide is grown on the exposed sidewall of the deep trench DT to form ~~trench~~ the gate oxide layer 24 of the vertical array FET transistor 17.

[0066] (13) As in FIG. 3, an angled ion implantation of an N-type dopant species at an a greater angle $\theta + \delta$ with respect to vertical is made through the exposed gate oxide layer 24 in recess R and into the deep trench sidewall to form N-type doping pockets. The N-type dopant can be either phosphorus (P) or arsenic (As), with arsenic being the preferred dopant because of the heavy mass thereof. The preferred energy for ion implantation of arsenic into the channel region CH is about 10 keV, in order to avoid overcompensation of the P-type V_t adjustment doping with dopant 32.

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[0067] Another angled ion implantation of P-type dopant 32 at a lesser angle θ with respect to vertical is subsequently made through the recessed polysilicon of the gate conductor 16 and the sidewall of deep trench DT and gate oxide layer 24. Since both implants are self-aligned to the edge of the gate conductor 16, a p-n junction is formed and self-aligned to the gate edge as well. The implant species, energy and dose are chosen such that the junction is placed just below the level 40 of the recessed GC edge and the threshold voltage V_t is sufficient to suppress sub-threshold leakage current. Preferably, the lesser angle θ is about 7° and the greater angle $\theta + \delta$ is about 30° .

[0070] While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with modification ~~modific~~ within the spirit and scope of the appended claims, i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the claims which follow.